RAMAKRISHNA MISSION VIDYAMANDIRA

(A Residential Autonomous College under University of Calcutta)

First Year

First-Semester Examination, December 2010

Date : 18-12-2010 **ELECTRONICS (General)** Full Marks : 50

Time : 10am – 12noon **Paper - I**

Answer <u>any five</u> questions : [5×10 = 50]

1. a) Subtract decimal number 25 from 49 using 2's complement method.
   b) Starting from the expression Y = A´B + AB´, simplify it to draw the circuit by using NOR gates only.
   c) If the voltage measuring range of a digital voltmeter is 0 to 10V and 16 bit encoding is used, then what will be the resolution in voltage reading? [3+3+4 = 10]

2. a) Realize the function F = ∑m(0, 1, 4, 5, 7) using 4:1 MUX.
   b) Write the truth table of a full adder and draw the circuit by using NAND gates only.
   c) Convert the decimal number 156·7 into BCD. [4+4+2 = 10]

3. a) If X = ABC + AB´C´ + A´BC´ and Y = (A´+B´+C´)(A´+B+C)(A+B´+C); then find the relation between X and Y?
   b) What is decoder? Explain the operation of BCD to binary decoder. [3+(2+5) = 10]

4. a) What is race-around problem for J-K flip-flop? How can it be avoided?
   b) Design a circuit that divides a clock to 1/8th of its initial frequency using J-K flip flops.
   c) State the difference between latches and flip flop. [(2+2)+3+3 = 10]

5. a) Design a counter that counts 0, 2, 4, 3, 9, 10, 13 in this order using all JK flip-flops. Explain the operation.
   b) What is shift register? Explain the operation of a 4-bit PISO shift register. [4+(2+4) = 10]

6. a) Define Fan-in and Fan-out in digital circuitry.
   b) How are the synchronous counters more advantageous than asynchronous counters? Explain.
   c) Design a 4:1 MUX using NAND gates only. [(1½×2)+5+2 = 10]

7. a) Design a 16:1 MUX using 4:1 MUXs and basic gates and explain the operation.
   b) Illustrate about different uses of MUX and DEMUX. [6+4 = 10]